REMARKS/ARGUMENTS

The Examiner found that claims 3-7 and 13-17 would be allowed if rewritten in independent form. Applicants submit that these claims are patentable over the cited art in their current form because they depend from one of base claims 1, 11, and 21, which are patentable over the cited art for the reasons discussed below.

The Examiner rejected claims 1, 2, 8-12, 18-22, and 28-30 as anticipated (35 U.S.C. §102(e)) by Sano (U.S. Patent No. 6,912,602). Applicants traverse with respect to the amended claims.

Amended claims 1, 11, and 21 recite processing packets from an Input/Output (I/O) device, and require: maintaining information indicating a different pair of a first buffer and a second buffer assigned to each of a plurality of descriptors, wherein one of the first and second buffers ~~is~~ assigned to one descriptor is used by the I/O device, and wherein the I/O device write packets to the buffers assigned to the descriptors; accessing the first buffer including a packet from the I/O device, wherein the accessed first buffer is assigned to an accessed descriptor that is one of the plurality of descriptors; processing the packet in the accessed first buffer; and if the second buffer assigned to the accessed descriptor is available, then updating information for the accessed descriptor to indicate that the second buffer is assigned to the accessed descriptor before completing the processing of the packet in the first buffer.

In the Examiner Interview Summary Record dated May 12th, the Examiner suggested "trying to distinguish that the first and second buffer are a PAIR of buffers that can be assigned to the same descriptor in order to help separate claims from Sano et al." Applicants amended the independent claims to clarify that a different pair of a first and second buffer pair are assigned to each of a plurality of descriptors. Applicants further clarified that one of the buffers assigned to one descriptor is used by the I/O device and that the accessed descriptor is one of the plurality of descriptors. These amendments are disclosed on at least para. [0008] on pgs. 3-4 and FIG. 1.

The Examiner cited FIG. 5 and elements 86 and 92 as teaching buffers for use with a descriptor. (Office Action, pg. 3) Applicants traverse.

The cited descriptor buffer 86 stores the descriptor for a packet in the PDI 40 circuit, which is a input packet DMA circuit to transmit write commands on the interconnect 22 to write received packets to memory. The descriptor buffer 92 stores the descriptor for a packet in the

PDO 42 circuit, which is an output packet DMA circuit to transmit read commands on the interconnect and to receive the read data of packets to be transmitted from the system. (Sano, col. 6, lines 15-26 and col. 10, lines 51 to col. 11, line 7). The control circuit 84 of the PDI generates read commands to prefetch descriptors into the descriptor buffer and generate write commands to write data from the input buffer to the memory buffer and to write the descriptor back to memory after the descriptor has been used to store packet data. (col. 11, lines 55-67). The control circuit 90 in the PDO may prefetch one or more descriptors into the descriptor buffer 92. (col. 12, lines 23-39)

Nowhere does the cited Sano anywhere disclose a different pair of first and second buffers assigned to each of a plurality of descriptors, where the buffers store the packet for the descriptor. Instead, the buffers 86 and 92 are used to store descriptors of data being written from the input buffer 88 and read into the output buffer 94. Although the buffers 86 and 92 store descriptors for packets being stored in buffers 88 and 94, there is no disclosure in the cited Sano of the claim requirements of a different pair of buffers for each of a plurality of descriptors. Instead, the cited buffers 86 and 92 store descriptors, not packets to the buffers assigned to the accessed descriptor as claimed.

The Examiner cited various parts of Sano, including elements 92 and 16 in FIGs. 1 and 5 as disclosing the claim requirement that if the second buffer assigned to the accessed descriptor is available, then updating information for the accessed descriptor to indicate that the second buffer is assigned to the accessed descriptor before completing the processing of the packet in the first buffer. (Office Action, pg. 4) Applicants traverse.

The cited element 92 comprises the buffer in the PDO, which transmits read commands. The cited element 16 is the DMA circuit that communicates packets between the interface circuits and the memory, and may generate write commands to the memory controller to write packets to the memory and generate read commands to read packets from the memory for transmission by one interface circuit. (Sano, col. 3, lines 34-40).

Although the cited Sano discusses how a DMA circuit transmits packets between interface circuits and memory, nowhere is there any disclosure or mention of the claim requirement that if the second buffer assigned to the accessed descriptor is available, then updating information for the accessed descriptor to indicate that the second buffer is assigned to the accessed descriptor before completing the processing of the packet in the first buffer. The

Examiner has not cited any part of Sano that discloses updating information in the accessed descriptor to indicate that the second buffer is assigned to the descriptor before completing the processing of the packet in the first buffer.

Further, although the cited buffers 86 and 92 store descriptors, the Examiner has not cited any part of Sano that information for the accessed descriptor is updated to indicate that the second buffer of the pair assigned to the descriptor is updated before completing processing of the packet in the first buffer.

Accordingly, amended claims 1, 11, and 21 are patentable over the cited art because the cited art does not disclose the requirements of these claims.

Claims 2, 8-10, 12, 18-20, 22, and 28-30 are patentable over the cited art because they depend from one of claims 1, 11, and 21, which are patentable over the cited art for the reasons discussed above.

Amended claims 9, 19, and 29 depend from claims 1, 11, and 21, respectively, and additionally require that there are at least two buffers assigned to each descriptor. This requirement is disclosed on at least FIG. 1 and para. [0008] of the Specification, which disclose multiple buffers for each descriptor.

Conclusion

For all the above reasons, Applicant submits that the pending claims 1-30 are patentable over the art of record. Applicants have not added any claims. Nonetheless, should any additional fees be required, please charge Deposit Account No. 50-0585.

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The attorney of record invites the Examiner to contact him at (310) 553-7977 if the Examiner believes such contact would advance the prosecution of the case.

Dated: May 23, 2006

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